REMARKS

The Office Action dated February 23, 2005, was carefully reviewed. The Examiner rejected claims 1-9 under 35 U.S.C. § 103(a) as being anticipated by U.S. Patent No. 6,138,185 to Nelson et al., hereinafter Nelson in view of U.S. Patent No. 6,745,271 B2 to Toda.

The Examiner asserted that Nelson discloses all of the limitations of claim 1 except synchronizing the serial I/O shifter using the clock signal. The Examiner asserted that Toda discloses clock lines being input to each of the memory modules and the controller, data input/output operations of each of the memory and the controller being performed in synch with basic clocks. The Examiner asserted that it would have been obvious to combine Nelson with Toda to achieve the present invention.

The present invention requires a clock signal for clocking a transfer of serial data from the controller to the external device. The clock signal is for synchronizing the operation of the serial I/O shifter. The present invention teaches reconstructing serialized data for communication with a parallel device. Parallel reconstruction begins on the assertion of a latch signal to the external device. Thereafter, serial I/O data from the external device is clocked into the serial I/O shifter. Once all "n" bits of the serial I/O data stream have been clocked into the shifter, the shifter reconstructs the serial data into parallel I/O signals. The parallel I/O signals are then output to the I/O crossover-switching network.

According to the present invention, the operation of all of the serial I/O shifters is synchronized to their respective SCLK and SLATCH signals. As a result, when more than one shifter is associated with a *single* clock and latch signal, data of all the serial I/O shifters related to that particular SCLK signal and SLATCH signal are serialized, and de-serialized, in parallel.

The Toda reference is directed to fast data transfer between memory modules and a controller. The Toda reference attempts to solve the problem of data collisions on a data bus. The Toda reference proposes a fast data transfer system that permits data transfers at high speed without the need for additional data buses.

The Toda reference teaches a fast data transfer system that requires a plurality of memory modules, a controller and first and second basic clock cycles. Toda teaches a first basic clock and a second basic clock having a cycle that is 2 or 4 times longer than the first basic clock cycle. The clock cycles taught by Toda work in combination with each other in order to avoid data collisions on the data bus. The Toda reference does not teach or disclose a single clock signal for synchronizing the operation of a serial I/O shifter as taught by the present invention.

In Toda, the two clock lines are arranged so that they go and return. The first and second basic clocks control data transfer, but do not synchronize the operation of a serial I/O shifter. After passing through the turnaround point, the first and second basic clocks are transferred as return clocks. The clocks do not control data operations, the controller 3 controls the respective

data input/output operations by making data transfers on the basis of currents of given magnitude flowing therethrough which synchronizes when to write data and when to read data with the first and second basic clocks. According to Toda, (column 7, lines 8-11), each memory module receives an address/command at timing B and then outputs data onto the data bus after a fixed number of clock cycles from timing A.

Toda does not teach or disclose a single clock signal for synchronizing the operation of at least one serial I/O shifter as claimed by the present invention.

It is respectfully asserted that one skilled in the art would not look to combine the two references as suggested by the Examiner. The present invention teaches a single clock cycle to synchronize the serial I/O shifter. The Nelson reference teaches a clock signal to encode requests and the Toda reference teaches the combination of first and second clocks working together, with different cycle periods to avoid data collisions. One skilled in the art would not look to combine these references to achieve synchronization of a serial I/O shifter by a single clock cycle as taught by the present invention.

It is respectfully asserted that even if the references were combined as suggested by the Examiner, the combination would not result in the applicants' invention. The combination of Nelson and Toda would result in a dual clock signal that is used to process connection and clear requests concurrently to avoid blocking signals at busy ports.

Regarding claim 5, the present invention teaches serially transferring bits of the data stream from an I/O multiplexer to an external device at the rate of one bit per cycle of a clock signal. This is neither taught, nor disclosed, in Toda and Nelson, and therefore cannot possibly be taught or disclosed in their combination.

Regarding claim 5, and the claims that depend therefrom, the Examiner reiterated the assertion that Nelson discloses serially transferring bits of the data stream from an I/O multiplexer to an external device at the rate of one bit per cycle of a clock signal at column 3, line 64 to column 4, line 30. t is respectfully asserted that Nelson does not teach or disclose transferring bits of the data stream at the rate of one bit per cycle of a clock signal and does not teach or disclose transferring bits of the data stream from an I/O multiplexer to an external device at the rate of one bit per cycle of a clock signal.

The Nelson reference discloses a serial crossbar controller. Further, at column 4, lines 5-17, Nelson emphasizes that each serial request bus and each serial reply bus are independent, requests and responses can be processed concurrently to reduce latency. Nelson defines "concurrently" as meaning all requests are "processed during a single clock cycle." It is respectfully asserted that this is significantly different than processing each request during a single clock cycle as asserted by the Examiner. The clock signal in Nelson is not used to serialize parallel data and does not serially transfer bits of the data stream to an external device at the rate of one bit per cycle as taught by the Applicant of the present invention.

It is respectfully requested the Examiner withdraw the rejection of claims 1-9 under 35 U.S.C. § 103. Should the Examiner have any questions or comments that may place the application in better condition for allowance, he is respectfully requested to call the undersigned attorney.

Respectfully submitted,

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